Example 3: Uncovering Geographic Issues at Final Test

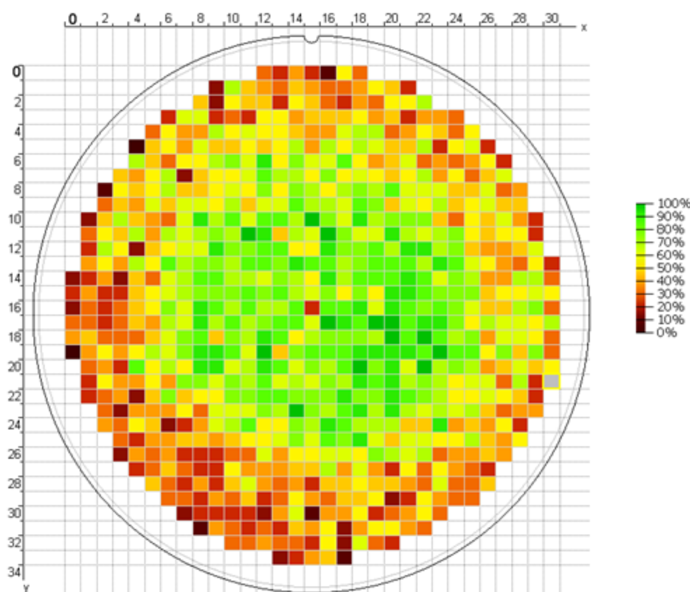
Finding the Issue

When a chip has an Electronic Chip ID (ECID) it is possible to discover wafer geography issues based on final test data. Even though parts pass at wafer sort, they fail at final test and the fallout is related to wafer geography and fab process issues. The trigger for performing this analysis is a final test parametric test that has a higher than expected failure rate. This is discovered using a failing test Pareto chart in the Optimal+ solution's portal.

Performing the Analysis

In this example, an engineer uses the solution's wafer map reconstruction capabilities to analyze the fallout of a parametric test performed at final test. Wafer map reconstruction is an excellent tool for yield learning analysis. The wafer clearly shows that most of the failures occur near the edge of the wafer. The impact of this issue is that failures, which could be detected at wafer sort, were deferred to final test, causing costly and unnecessary packaging of bad devices.

This issue is resolved by creating a screening test in the wafer sort process so that these problems are caught earlier. The fab is notified so that improvements can be made to the wafer manufacturing process. We call this useful capability "Data Feed Backward" – taking data from a later operation and using it for yield learning in earlier operations.



For more information please contact Optiaml+ team at info@optimalplus.com